UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,712	09/29/2003	Lawrence Salant	455610-2580.1	2458

20999 7590 06/07/2006

FROMMER LAWRENCE & HAUG
745 FIFTH AVENUE- 10TH FL.
NEW YORK, NY 10151

EXAMINER	
MERANT, GUERRIER	

ART UNIT	PAPER NUMBER
2191	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/673,712	SALANT ET AL.	
	Examin r	Art Unit	
	Guerrier Merant	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for R ply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09/29/03*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09/29/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is the initial office action based on the application filed on September 29, 2003.

Claims 1-18 are currently pending and have been considered below.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3,5,6,8-12,14,15,17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Verboom (US 20010021151 A1).

Claim 1: Verboom discloses a method for determining a bit rate, comprising the step of:

a) acquiring a data signal by an acquisition unit of a test instrument for a predetermined period of time (abstract & [0091]);

b) storing said data signal in a memory (register) of said test instrument [0133] & [0084];

c) recovering a clock signal from said stored data signal [00069];

d) slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered clock signal (abst. "sampling the read signal at channel bit locations to provide a plurality of samples") & [0091]-[0094];

e) synchronizing each of said data segments to align them to a frame or predetermined pattern to determine a bit error rate [0034]&[0037]-[0045] &[0068]-[0070];

f) and comparing each of said data segments to said predetermined pattern on a bit by bit basis [0007]-[0092].

Claim 2: Verboom discloses a method of processing a data signal as in claim 1 above, wherein said clock recovery step further comprises the steps of:

a) defining a threshold level relative to said stored data signal [0006]-[0013] & [0093];

b) comparing each portion of the stored data signal to said threshold level [0006]&[[0093];

c) determining pairs of adjacent samples that straddle said threshold [0105];

d) and estimating a time of crossing said threshold between said adjacent samples to obtain a series of observed times of threshold crossing. [0006] -[0131].

Claim 3: Verboom discloses a method as in claim 2 above, wherein said clock recovery step further comprising the steps of:

a) comparing said series of observed times of threshold crossing to an ideal perfectly periodic sequence of expected times of threshold crossing comprising said recovered virtual periodic clock [0006]-[0013]

b) determining an error between said observed times of threshold crossing and of said series of expected times of threshold crossing comprising said recovered virtual clock based upon said comparison [0006]-[0013];

c) and adjusting the phase of said recovered virtual periodic clock in accordance with said determined error [0012]-[0090].

Claim 5: Verboom discloses a method as in claim 1 above, wherein said predetermined pattern is compared to each of said data segments to determine bit errors therein [0007]-[0008] &[0092].

Claim 6: Verboom discloses a method as in claim 5 above, wherein if said determined bit rate is extremely high above a predetermined threshold, said alignment between the pattern and the data segments is adjusted [0007]-[0009].

Claim 8: Verboom discloses a method as in claim 1 above, wherein said predetermined pattern is a known standard test pattern [0008] & [0092].

Claim 9: Verboom discloses a method as in claim 1 above, wherein said predetermined pattern is a custom test pattern stored in a data file [0007]-[0031].

Claim 10: Verboom discloses an apparatus for determining a bit rate, comprising the step of:

a) acquiring a data signal by an acquisition unit of a test instrument for a predetermined period of time (abstract & [0091]);

b) storing said data signal in a memory (register) of said test instrument [0133] & [0084];

c) recovering a clock signal from said stored data signal [00069];

d) slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered clock signal (abst. "sampling the read signal at channel bit locations to provide a plurality of samples") & [0091]-[0094];

e) synchronizing each of said data segments to align them to a frame or predetermined pattern to determine a bit error rate [0034]&[0037]-[0045] &[0068]-[0070];

f) and comparing each of said data segments to said predetermined pattern on a bit by bit basis [0007]-[0092].

Claim 11: Verboom, Johannes J discloses a the apparatus as in claim 10 above, wherein said clock recovery step further comprises the steps of:

a) defining a threshold level relative to said stored data signal [0006]-[0013] & [0093];

b) comparing each portion of the stored data signal to said threshold level [0006]&[[0093];

c) determining pairs of adjacent samples that straddle said threshold [0105];

d) and estimating a time of crossing said threshold between said adjacent samples to obtain a series of observed times of threshold crossing. [0006] -[0131].

Claim 12: Verboom, Johannes J discloses a method as in claim 11 above, wherein said clock recovery step further comprising the steps of:

a) comparing said series of observed times of threshold crossing to an ideal perfectly periodic sequence of expected times of threshold crossing comprising said recovered virtual periodic clock [0006]-[0013]

b) determining an error between said observed times of threshold crossing and of said series of expected times of threshold crossing comprising said recovered virtual clock based upon said comparison [0006]-[0013];

c) and adjusting the phase of said recovered virtual periodic clock in accordance with said determined error [0012]-[0090].

Claim 14: Verboom discloses the apparatus as in claim 10 above, wherein said predetermined pattern is compared to each of said data segments to determine bit errors therein [0007]-[0008] &[0092].

Claim 15: Verboom discloses the apparatus as in claim 14 above, wherein if said determined bit rate is extremely high above a predetermined threshold, said alignment between the pattern and the data segments is adjusted [0007]-[0009].

Claim 17: Verboom discloses an apparatus as in claim 10 above, wherein said predetermined pattern is a known standard test pattern [0008] & [0092].

Claim 18: Verboom discloses an apparatus as in claim 10 above, wherein said predetermined pattern is a custom test pattern stored in a data file [0007]-[0031].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a

whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Verboom

Claim 4: Verboom discloses a method as in claim 1 above, further comprising the steps of determining a position of each bit error in a frame ([0135] & FIG. 3 showing x/y coordinate) but does not disclose displaying the data to a user. At the time of the invention it would have been obvious to a person of ordinary skill in the art to display Verboom x/y coordinate data to the user. One would have been motivated to display the data in order to allow a user to make adjustment.

Claim 13: Verboom discloses a method as in claim 10 above, further comprising the steps of determining a position of each bit error in a frame ([0135] & FIG. 3 showing x/y coordinate) but does not disclose displaying the data to a user. At the time of the invention it would have been obvious to a person of ordinary skill in the art to display Verboom x/y coordinate data to the user. One would have been motivated to display the data in order to allow a user to make adjustment.

Claims 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Verboom in view of Tomita (US 20020023243 A1).

Claim 7: Verboom discloses a method as in claim 1 above, but did specify that the predetermined pattern is a pseudo-randomly generated bit sequence.

However, Tomita discloses a pseudo-randomly generated bit rate that is used to identify bit error rate [0005], [0016] & [0042].

Verboom and Tomita are analogous arts because they are from the same field of endeavor of error detection and correction.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Verboom and a pseudo-randomly generated bit sequence in order to identify bit error rate as disclosed in Tomita.

Claim 16: Verboom discloses a method as in claim 10 above, but did specify that the predetermined pattern is a pseudo-randomly generated bit sequence.

However, Tomita discloses a pseudo-randomly generated bit rate that is used to identify bit error rate [0005], [0016] & [0042].

Verboom and Tomita are analogous arts because they are from the same field of endeavor of error detection and correction.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Verboom and a pseudo-randomly generated bit sequence in order to identify bit error rate as disclosed in Tomita.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Miyashita et al. (US 6922384 B2) discloses an apparatus for reproducing information that has been written on a storage medium such as an optical disk or a magnetic disk.

b) Seng et al. (US 20020128787 A1) discloses System and method to determine the time domain equalized signal-to-noise ratio of a mass storage device.

c) Shekter et al. (US 20020034337 A1) discloses a system for manipulating noise in digital images.

d) Rhoads et al. (US 20020018572 A1) discloses Methods for detecting alteration of audio.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 5:30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Myhre, can be reached on (571) 270-10765. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-1066.

M. G.

M.G.

09/17/06

James W. Myhre

Supervisory Patent Examiner